Journal of Engineering Research and Reports

12(2): 37-45, 2020; Article no.JERR.56482
ISSN: 2582-2926

Non-stick on Pad Defect Reduction through Clamp and Insert Design Augmentation

Antonio Sumagpang Jr.[1*], Rennier Rodriguez[1] and Frederick Ray Gomez[1]

[1]New Product Development & Introduction Department, STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2020/v12i217078
Editor(s):
(1) Dr. Ravi Kant, Maharaja Ranjit Singh Sate Technical University, India.
(2) Er. Anuj Kr. Goel, Maharishi Markandeshwar University, India.
Reviewers:
(1) Raheel Muzzammel, University of Lahore, Pakistan.
(2) Rohit L. Vekariya, CVM University, India.
Complete Peer review History: http://www.sdiarticle4.com/review-history/56482

Original Research Article

Received 21 February 2020
Accepted 27 April 2020
Published 04 May 2020

ABSTRACT

With new and continuous technology development and breakthroughs, few to several challenges in semiconductor assembly manufacturing are inevitable. One critical assembly process often affected with these technology trends and changes is the wirebond process. In due course, this paper focused on the elimination of non-stick on pad (NSOP) assembly defect at the wirebond process. Fishbone analysis and why-why analysis were done to comprehensively investigate the root-cause and eventually address the problem. High NSOP rejection rate was identified to be attributed to clamp and insert design, and was verified through series of analysis, design of experiment (DOE) and validation runs. Results revealed that by using the modified clamp and insert design with more holes would address NSOP rejection with around 90% defect reduction.

Keywords: NSOP; wirebond; clamp and insert; assembly.

**Corresponding author: Email: antonio.sumagpang@st.com;*

1. INTRODUCTION

One of the biggest challenges for semiconductor manufacturing companies is to maintain its competitive market position and value. New technology has provided manufacturability challenges and one particular process mostly affected is the wirebonding process. During package development stage of a semiconductor chip-on-lead package, one major challenge needs to be addressed is the non-stick on pad (hereinafter referred to as NSOP) or the non-adhering of the wirebond ball to the silicon die's bond pad. An actual photo of the NSOP defect on the device in focus is given in Fig. 1. Notice on the red arrow that the bond pad has no bondwire (or simply wire) connected or bonded to it, where it should have been an electrical connection. NSOP would subsequently result to an open-circuit for that particular signal, ultimately disabling the functionality of the device.

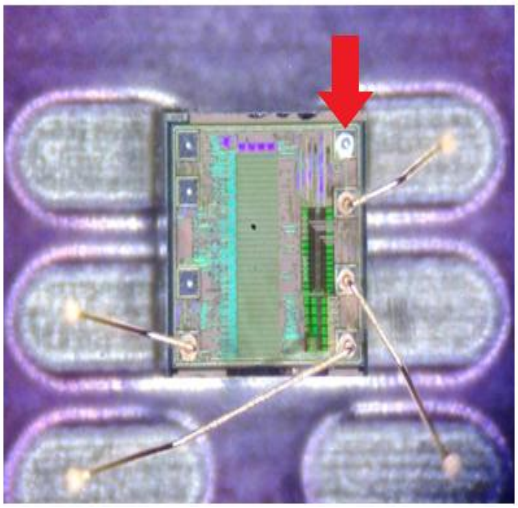


Fig. 1. NSOP defect

With new and continuing technology trends and state-of-the-art platforms [1,2], this paper discussed how the challenges were turned into milestones when top yield detractors of critical processes were addressed by in-depth engineering analysis and utilizing statistical tools at early stage of production.

2. LITERATURE REVIEW AND PROBLEM IDENTIFICATION

Wirebond process is one of the challenging processes in semiconductor manufacturing industry responsible in attaching the wires to provide electrical connections through combination of heat, pressure and thermosonic energy. The wire used in wirebonding is usually made either of Gold (Au) or Aluminum (Al), although Copper (Cu) wires are starting to gain attention in the semiconductor manufacturing industry [3-5]. For the device in focus, copper wirebonding is used.

During initial phase of the investigation, all possible variables to determine the yield loss contributors were studied [2,6,7]. The entire processes were analyzed as this product carries new process bricks and technology for the plant such as copper wirebonding and the use of tapeless leadframe which is more sensitive than the conventional leadframe. An overview of the assembly process flow is shown in Fig. 2. It is worth noting that process flow varies with the product and the technology [8-10]. As earlier stated, with new and continuous technology trends and breakthroughs, challenges in semiconductor assembly manufacturing are inevitable.

During the investigation, it was established that the major source of yield loss during ramp-up stage is wirebond. This is a substantial finding so that attention and effort for the root-cause analysis will only focus on this process. Furthermore, yield detractors and top defects were also identified by collecting defect signatures that will serve as lead to further investigate and analyze the root-cause of the problems.

In order to have a lead on the problems for each process, actual defects were collected, studied and analyzed deeper based on defect signatures. Shown in Table 1 is the defect signature of NSOP during wirebond process.

Several lots during ramp-up in production were severely affected and way above the allowable parts per million (ppm). Fig. 3 shows the rejection rate of NSOP over a particular period in time.

NSOP rejection rate is classified as wirebonding-related defects that provided significant failure affecting the assembly yield during ramp-up stage of the device. Most of the process batches were put on-hold and visually inspected due to alarming high rejection rate. This triggered the team to deep dive onto the problem, identify the root-cause, and come-up with the best solution.

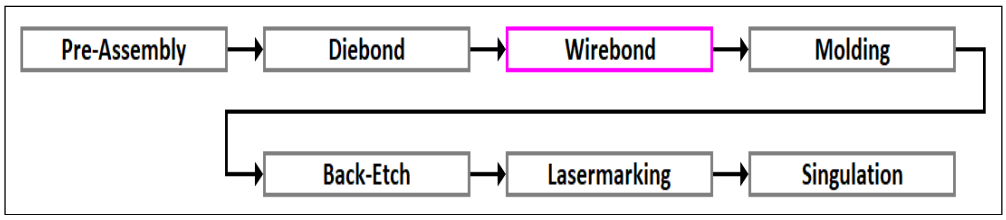
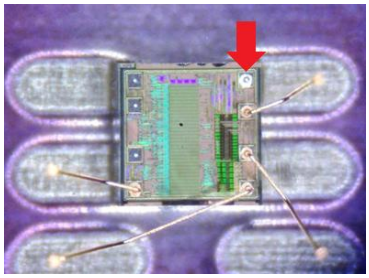


Fig. 2. Assembly process flow

Table 1. Ball shear and wire pull test results

Defect signature	Defect call-out	Defect mechanism	Remarks
	NSOP	Ball not adhered to bond pad	Reject

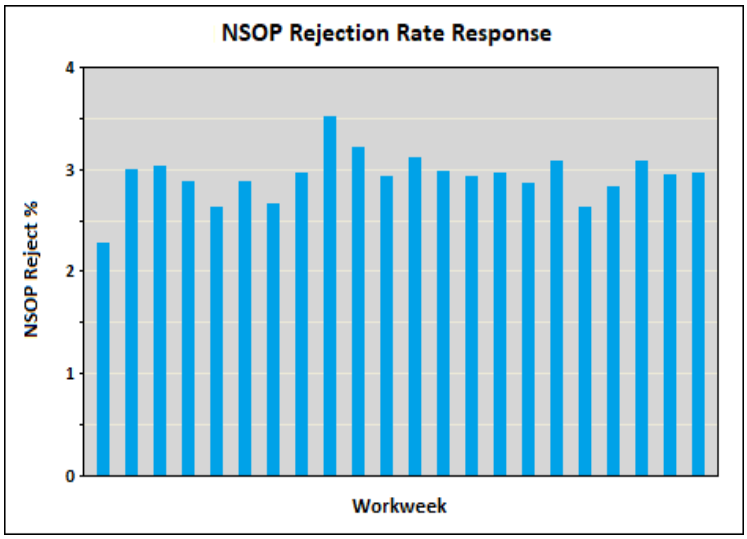


Fig. 3. NSOP rejection rate

3. METHODOLOGY

To capture all variables or potential causes leading to NSOP, fishbone diagram in Fig. 4 and cause and effect analysis were employed. Each cause was validated to come up to the true causes, with validations made as shown in Table 2.

Actual photos of bonded units showing NSOP manifestation are shown in Fig. 5, with the defect occurring in one of the bond pads of the device' silicon die.

Machine-to-machine validation was also performed to check if NSOP defect is not machine related. The same diffusion wafer batch was split into three wirebonding machines but gave the same results and level of NSOP rejects. With that, wirebond machine was set aside in the investigation.

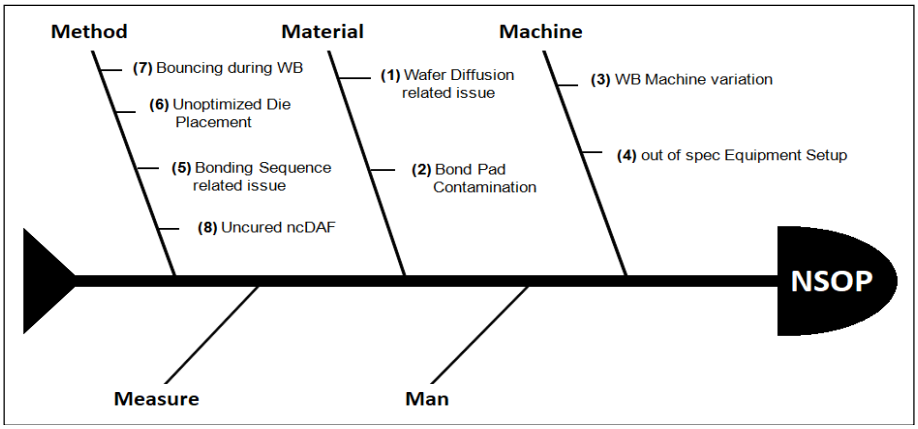


Fig. 4. Fishbone diagram

Table 2. Validation of potential causes

Potential cause		Method of validation	Result of validation	Conclusion
1	Wafer diffusion	Check if problem is isolated on a specific diffusion	All diffusions are affected by NSOP	Not True Cause
2	Bond pad contamination	Perform Energy-Dispersive X-ray Spectroscopy (EDX) analysis on affected pads	No contamination detected	Not True Cause
3	Wirebond machine variation	Check machine1 and machine2 for NSOP response	Both machines manifest NSOP occurrences	Not True Cause
4	Out of specification equipment setup	Check equipment parameters	Pertinent parameters within specification	Not True Cause
5	Bonding sequence related issue	Compare NSOP occurrence when reverse bonding sequence is used	NSOP is encountered at 7/30 units	Not True Cause
6	Un-optimized die placement	Optimize die placement through Design-of-Experiment (DOE)	NSOP is encountered at 6/30 units	Not True Cause
7	Bouncing during wirebonding	Use high-speed camera to check manifestation of bouncing at pad area during wirebond	Bouncing phenomenon observed: 8/30 NSOP is due to clamp and inserts	True Cause
8	Uncured non-conductive die attach film	Check the Differential Scanning Calorimetry (DSC) of material	Non-conductive die attach film is fully cured	Not True Cause

Further in-depth analysis and validation was made through why-why analysis shown in Table 3. This confirmed that the configuration of the designed insert used during the line stressing lot of the device is causing the NSOP rejection.

More holes on the insert would avoid air traps in between units and eventually flatten the leadframe during vacuum at wirebonding. Fig. 6 compares the previous and the new insert designs.

A flattened leadframe results to better wire bond quality and less probability of NSOP occurrence. Table 4 provides the why-why analysis of systematic root-cause. Escape root-cause is not anymore applicable since NSOP was effectively detected by the current control (alarm) during wire bond.

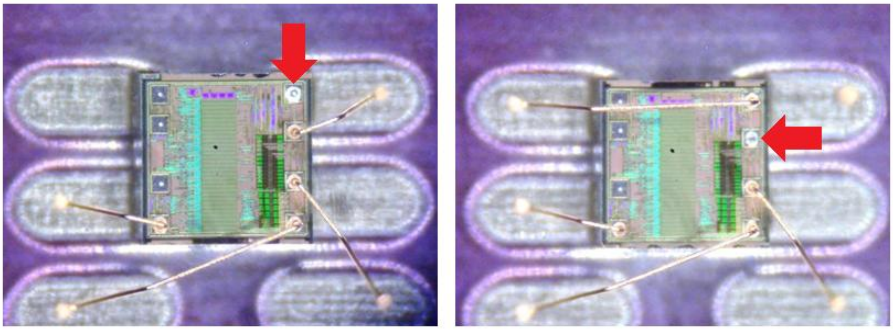


Fig. 5. NSOP defect mechanism

Table 3. Technical root-cause why-why analysis

Why 1	Why 2	Why 3	Why 4	Why 5	Why 6
Bouncing on leadframe pad area during wirebond resulting to NSOP	Leadframe pad area is not firmly hold upon vacuum activation after panel clamping	Presence of entrapped air between leadframe and insert	Air is not able to escape through the designed holes in the insert	Vacuum holes are located too far apart (not fit for the device density)	It is the configuration of the designed insert used for the affected 2nd line stressing lot of the device

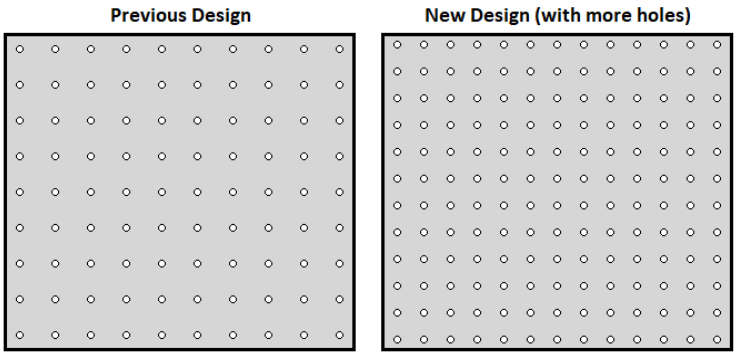


Fig. 6. Comparison of insert designs

Table 4. Systematic root-cause why-why analysis

Why 1	Why 2	Why 3	Why 4	Why 5
It is the configuration of the new insert used for the affected 2nd line stressing lot of the device	The configuration of the insert was designed by the supplier based on the LF drawing provided (in reference to the requested design change for the window clamp	As per current practice for clamp and insert design for new products		
	The change in insert configuration (from qualification to line stressing) was not detected upon delivery and use Focus is on the requested change in clam window opening	No incoming buy-off or inspection done for the new clamp and insert	Buy-off of clamp and insert not part of the procedure Only functional buy-off is done (on actual unit processing)	

4. RESULTS AND ANALYSIS

Results of comprehensive investigation through fishbone diagram and why-why analysis revealed that the root-cause of high NSOP rejection rate can be attributed to clamp and insert design, more specifically the insert design. This was identified after series of analysis and validation using different runs. The results were further strengthened by using a high speed camera that helped pinpoint the root-cause of the NSOP phenomenon. Results showed that by using the new and modified insert design with more holes, NSOP rejection would be addressed without sacrificing quality requirements of the products including reliability.

4.1 Clamp and Insert Design

A design-of-experiment (DOE) for 1st bond parameters was conducted with the objective to determine and define a window that will minimize occurrence of NSOP. Analysis of variance (ANOVA) in Fig. 7 revealed significant difference using new design and parameter over the previous design.

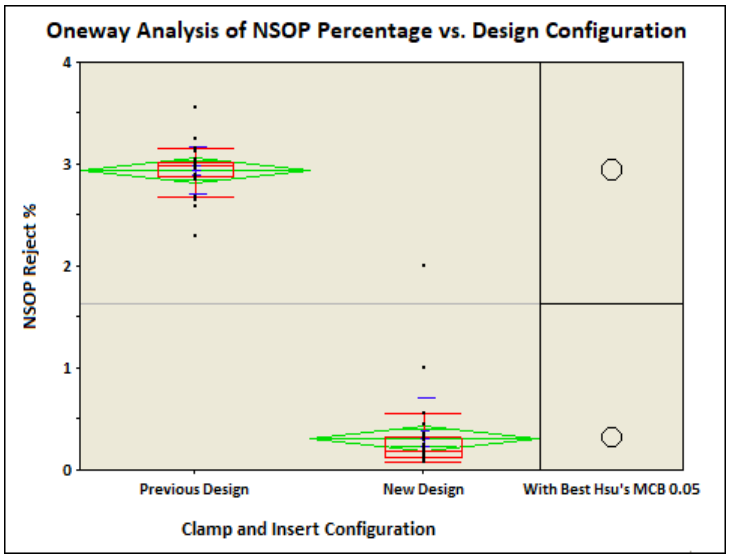


Fig. 7. Statistical analysis graph showing significant difference between the two designs

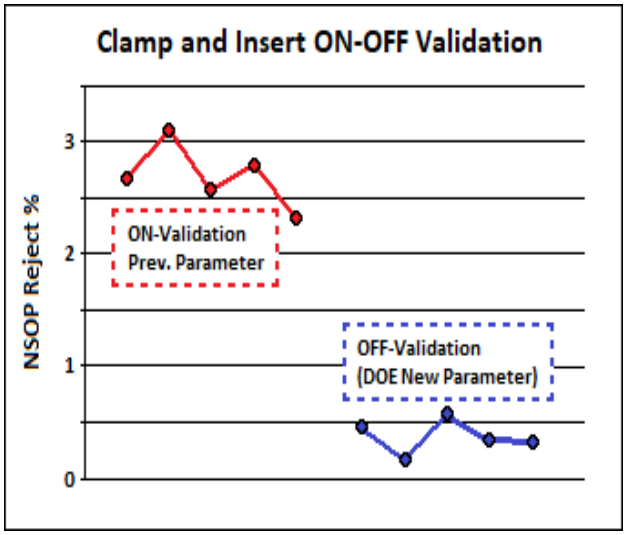


Fig. 8. On-off validation of clamp and insert designs

To strengthen the premise on NSOP is due to clamp and insert design. Wirebond parameters were brought back to its original setup. Employing On-Off validation, Fig. 8 depicts that new clamp and insert dictates the outcome of NSOP rejection rate. Results of all experiments and validation runs strengthened the conclusion that the NSOP due to poor design of clamp and insert could be mitigated using higher new design with enhanced vacuum capability.

4.2 Response on Critical Product Characteristics

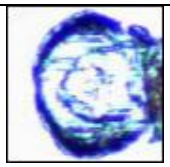
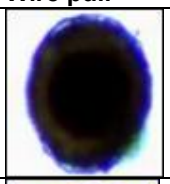
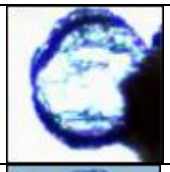
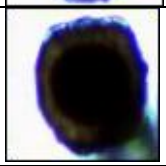
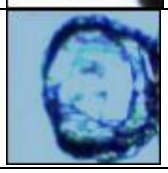
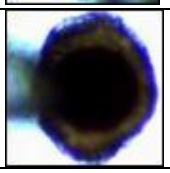
To further verify if the new set of parameters will satisfy the quality requirements based on the plant's standards, critical responses were studied and collected. Evaluation results are shown in Tables 5 and 6. Criteria for acceptance are governed by assembly process specifications and work instructions [11,12].

4.3 Solution Implementation

After replacement of new clamp and insert design that mitigates the risk of NSOP defects and validations in terms of quality and reliability aspects, large scale evaluations were made through line stressing to validate effectiveness of new clamp and insert design. Error-proofing was employed to identify actions that will either control or eliminate these errors.

Continuous monitoring on the lots during mass production was carried out. Result of verification, showed that the lot using new clamp and insert design has significantly lower rejection rate. NSOP trend together with the action and date of execution was monitored to confirm and validate the effectiveness of the implemented solution. Shown in Fig. 9 is the detailed monitoring graph regarding NSOP before and after the solution implementation.

Table 5. Ball shear and wire pull test results

Parameter	Ball shear	Wire pull	Remarks
Low side (LL)			Passed
Nominal (MID)			Passed
High side (HH)			Passed

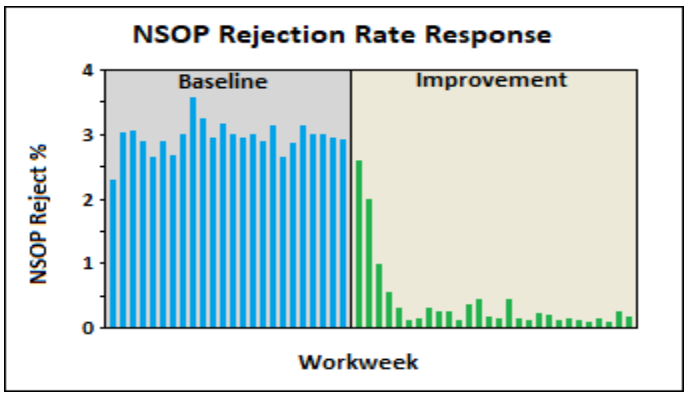
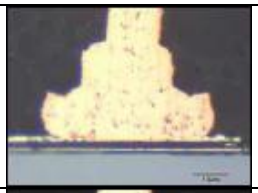
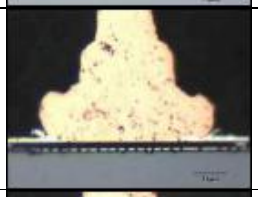


Fig. 9. NSOP performance after implementation of the new design

Table 6. Cross-sectional results

Parameter	Cross-section	Remarks
Low side (LL)		Passed
Nominal (MID)		Passed
High side (HH)		Passed

Assembly yield trend stabilized after the implementation, optimization, and sustainability of the improvement and all corrective actions.

5. CONCLUSION AND RECOMMENDATIONS

Comprehensive analysis coupled with statistical techniques was done to address the NSOP assembly issue. Using the knowledge and understanding on data and defect phenomena led to identify the true cause of the defect. In-depth why-why analysis and validation mitigated the NSOP rejects which are attributed to design of insert used during qualification affecting the performance copper wirebonding of the device. Through design modification of the clamp and insert, occurrence of NSOP rejects was significantly lessened with around 90% defect reduction. Ultimately, NSOP defect was solved without too much cost involved and no major alteration on the semiconductor assembly process.

Continuous process and design improvement are imperative to maintain high quality performance of semiconductor products and its assembly manufacturing. Studies and improvement done are helpful in reinforcing robustness and optimization of assembly processes.

ACKNOWLEDGEMENTS

The authors would like to thank the New Product Development & Introduction (NPD-I) team and colleagues of STMicroelectronics Calamba who have greatly contributed to the success of the work. The authors are also thankful to the Management Team for the continuous support.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan; 2002.
2. Sumagpang A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium, Philippines; 2012.
3. Tan CE, Liong JY, Dimatira J, Tan J, Kok LW. Challenges of ultimate ultra-fine pitch process with gold wire & copper wire in QFN packages. 36th International Electronics Manufacturing Technology Conference, Malaysia; 2014.
4. STMicroelectronics. Wire bonder capability in assembly plants. rev. 12; 2018.

5. Lall P, Deshpande S, Nguyen L. Reliability of copper, gold, silver and PCC wirebonds subjected to harsh environment. IEEE 68th Electronic Components and Technology Conference, San Diego, California, USA; 2018.
6. Rodriguez R, Gomez FR. Pick and place process optimization for thin semiconductor packages. Journal of Engineering Research and Reports. 2019;4(2):1-9.
7. Pulido J, Gomez FR, Graycochea Jr. E. Wirebond process improvement with enhanced stand-off bias wire clamp and top plate. Journal of Engineering Research and Reports. 2020;9(3):1-4.
8. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st Ed. Wiley-IEEE Press, USA; 2006.
9. Geng H. Semiconductor manufacturing handbook. 2nd Ed., McGraw-Hill Education, USA; 2017.
10. Nenni D, McLellan P. Fabless: The transformation of the semiconductor industry. CreateSpace Independent Publishing Platform, USA; 2014.
11. STMicroelectronics. Work instruction for wirebond monitoring. rev. 81; 2020.
12. STMicroelectronics. Assembly and EWS design rules for wirebond interconnect dice. rev. 53.0; 2018.

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sdiarticle4.com/review-history/56482