



# Die Attach Process Robustness through Epoxy Pattern Optimization for DFN Device

Jerome J. Dinglasan<sup>1\*</sup> and Frederick Ray I. Gomez<sup>1</sup>

<sup>1</sup>STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

## Authors' contributions

*This work was carried out in collaboration amongst the authors. Both authors read, reviewed and approved the final manuscript.*

## Article Information

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## ABSTRACT

As the modern world evolves through innovation and technology, manufacturing companies of semiconductor drive their people to dedicate themselves on continuous improvement and technical advancement. Products they produce becomes smaller and thinner, but applications are limitless and innovative. In manufacturing of quad flat no lead packages, challenges were encountered during the die attach process especially in small die size. Die attach material overflow on pad is one of these, and certain parameters and techniques are explored to have a quality and robust process. Defining appropriate epoxy pattern with respect to the die size is a big factor to make sure no epoxy material will flow outside the die pad perimeter that may cause unit rejection. This paper will discuss the related issues of the said package by performing experiments and applying certain techniques to address the problem.

*Keywords: DFN; die attach coverage; die attach process; epoxy; lead frame.*

## 1. INTRODUCTION

Semiconductor manufacturing had this one product design called DFN or dual-flat no-leads

packages used on surface mounting technology applications. This design does not utilize feet like "leads" like the conventional integrated circuits and are interconnected by either Gold (Au) or

\*Corresponding author: Email: [jerome.dinglasan@st.com](mailto:jerome.dinglasan@st.com);

Copper (Cu) wire during assembly. As seen on Fig. 1, package design with no leads is much more improved in terms of miniaturization, reduced lead inductance, and have improved thermal and electrical performance compared with conventional integrated circuits (IC) packages with leads.

In miniaturization of ICs, certain challenges have been encountered and determined at die attach [1-5]. This is the process of putting the silicon die with circuit design on a leadframe, dispensed with a die attach material (conductive/non-conductive epoxy) and will be subjected to oven curing. Epoxy dispensing on leadframe includes different pattern with respect to die size to achieve epoxy requirements, like area coverage, fillet height and the likes. If these requirements are not meant, possible problems are most likely to manifest, and product may be out of its designed function when used.

Epoxy overflow on pad is one of the challenges in manufacturing this DFN device and plays a big role in meeting the requirements of small die sizes. In epoxy dispensing, it is being considered and monitored that after placing the die, the epoxy flow should not exceed on the leadframe pad perimeter. If epoxy overflow on pad happens, it may cause unwanted rejects and affect other processes upstream of the manufacturing. Fig. 2 shows sample images of epoxy overflow on DFN packages that resulted to the yield loss and scrappage on the production.

## 2. METHODS AND RESULTS

Process flow of this quad flat no lead products starts with the process of wafer sawing on silicon wafer, cut into required size. Next step is the die attach process wherein singulated dice from wafers are picked and placed on a leadframe dispensed with die attach material (epoxy) and cured at a desired temperature. Interconnection comes next in the step of wire bonding process using wires made of Au or Silver (Ag) which serve as the connection of the circuit inside the

die to the leadframe. These processes are categorized as front-of-line (FOL) stations utilizing cleanroom environment, as the product is initially built on these steps, and the product is still open without encapsulation.

After the process on FOL, the product will now be encapsulated with a resin material, called mold process. Then this molded leadframe will now undergo curing at a certain temperature to cure the resin encapsulation. Singulation of the leadframe comes next to separate the wire bonded units individually. Marking as per requirement will be the next, placing a traceability and brand on the topside of the product. Series of inspections and tests will be performed before it will be delivered to the end customer. These processes are categorized as end-of-line (EOL) stations under a class 100k cleanroom.

The focus of the improvement will be on die attach station, and its epoxy dispensing aspects. Different epoxy patterns will be included on the experiment, with respect to the product's die size and will be the determining factor of the experiment. Three epoxy patterns are included in the experiment – the Double Y, Linear, and 3 Dots, as summarized in Table 1. Samples will be processed using these patterns and die attach responses will be gathered.

In performing this experiment on different epoxy patterns, we can see their difference through statistical analysis and their output response as we ought to resolve the phenomenon of epoxy overflow for the DFN package with small die.

Using statistical tools in this experiment, we can determine the desirable epoxy pattern with respect to its die size to address the epoxy overflow occurrence on manufacturing this package. Tally table of discrete variables in Fig. 3 shows initial data of 3 epoxy patterns using 30 samples including quantity and percentage of rejects. "Double Y" epoxy patterns have the most failed units at 40% on the given samples. Next is "3 Dots" and "line" epoxy patterns, respectively.

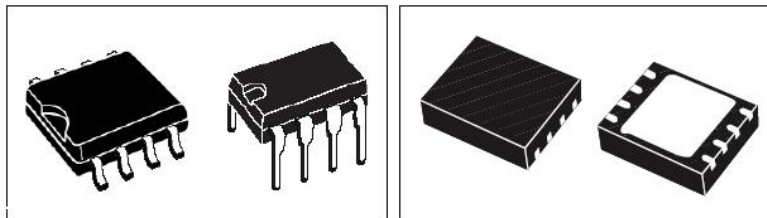


Fig. 1. Conventional package with leads (left); and DFN package (right)

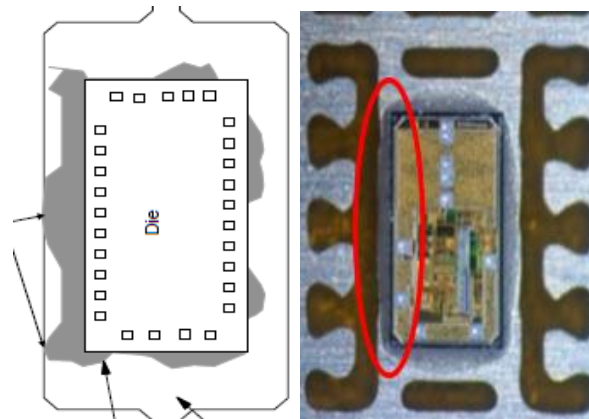


Fig. 2. Epoxy overflow on diepad

Tally for Discrete Variables: double Y, line, 3 dots

DOUBLE Y	double Y	Count	Percent
	fail	12	40
	Pass	18	60
	N=	30	

3 DOTS	3 dots	Count	Percent
	fail	2	6.67
	Pass	28	93.33
	N=	30	

LINE	line	Count	Percent
	Pass	30	100.00
	N=	30	

Fig. 3. Tally table of 3 different epoxy patterns

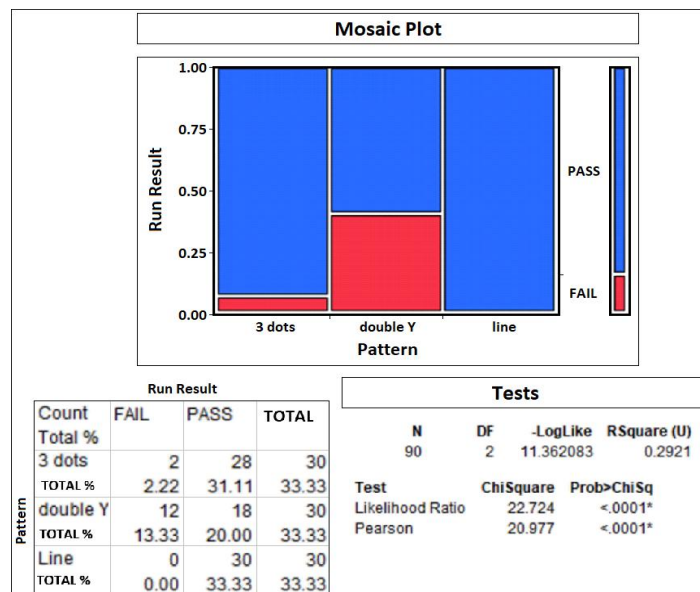
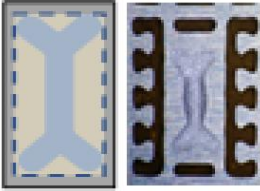
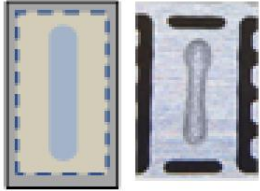
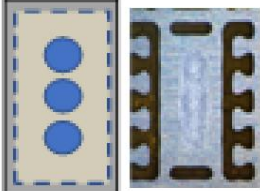


Fig. 4. Mosaic plot with statistical data interpretation

**Table 1. Experiment details**

Evaluation	Pattern	Pattern Image	Number of Samples
1	Double Y		30 units
2	Linear		30 units
3	3 Dots		30 units

Using statistical approach mosaic plot and chi square test in analyzing these 3 discrete variables, it shows that the “line” is the appropriate epoxy pattern to be used on this package. As seen on the statistical plots in Fig. 4, observations are taken in account:

- Experiment results differ between the variables (epoxy pattern)
- At better than 95% confidence level, using line pattern will result to much higher probability of no fail units

**3. CONCLUSION AND RECOMMENDATIONS**

Having shown on the statistical analysis performed on the experiment data the ideal epoxy pattern that gave positive results and eliminate the occurrence of epoxy overflow is the “line” pattern, as it projects the compatability of its design to match with the die size and die pad of the product making it more robust and efficient in manufacturing. Comparing with the other two patterns with rejection rate as computed, the said pattern is recommended to be applied on products having the same or almost near technical details and parameters. It is also being considered that continuous improvement and innovative ideas are essential to achieve a poka yoke oriented, efficient, and robust process of die attach in the semiconductor manufacturing. Works and learnings discussed in [6-11] would

help reinforce the robustness and optimization of die attach assembly process.

**DISCLAIMER**

The products used for this research are commonly and predominantly used products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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**COMPETING INTERESTS**

Authors have declared that no competing interests exist.

**REFERENCES**

1. Chin LS, et al. Epoxy die attach challenges in miniature and compact DFN/QFN packages. IEEE 10th Electronics

2. Tan CE and Fonseka G. QFN miniaturization: Challenges and solutions. International Electronic Manufacturing Technology (IEMT). Malaysia. 2006;314-319.
3. Rodriguez R, et al. Die attach process optimization with enhanced epoxy control on lead frame package. Journal of Engineering Research and Reports. 2020;14(2);32-37.
4. Abdullah S, et al. Dicing die attach film for 3D stacked die QFN package. 32nd IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). USA. 2007;73-75.
5. Xian TS and Nanthakumar P. Dicing die attach challenges at multi die stack packages. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT). Malaysia. 2012;1-5.
6. Buenviaje Jr. S, et al. Process optimization study on leadframe surface enhancements for delamination mitigation. IEEE 22nd Electronics Packaging Technology Conference (EPTC). Singapore. 2020;95-100.
7. Kahler J, et al. Pick-and-place silver sintering die attach of small-area chips. IEEE Transactions on Components, Packaging and Manufacturing Technology. 2012;2(2).
8. Sumagpang Jr. A and Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium. Philippines; 2012.
9. Graycochea Jr. E, et al. Package reliability performance study of QFN device on different die attach machines. Journal of Engineering Research and Reports. 2020;19(1);41-43.
10. Abdullah Z, et al. Die attach capability on ultra thin wafer thickness for power semiconductor. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference. Malaysia: 2012; 1-5.
11. Bacquian BC, et al. Bond line thickness characterization for QFN package robustness. Journal of Engineering Research and Reports. 2020;14(2):15-19.

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