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Introduction of Laser Pi-Grooving as Breakthrough Solution to Enhance die Strength of 40 nm ulow-k CMOS Silicon Technology during Wafer Saw Process

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Authors' contributions

This work was carried out in collaboration amongst the authors. All the authors read, reviewed and approved the final manuscript.

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ABSTRACT

Nowadays, semiconductors and electronics are becoming part of our everyday activities. As the Integrated circuits become more useful to people, it also requires more function, which contain more complex and compact components. Aligned to this package requirement, the more challenging it become to package development as Silicon technology becomes more critical and complex from bare silicon to conventional MOS technology to Ultra Low-K, which requires a different strategy. The new process development in the Semiconductor industry is a necessity to cope up with these new technologies. Low-k devices always pose a big challenge in achieving good dicing quality. This is because of the weak mechanical properties of the low-k dielectric material used. Mechanical Sawing is the most popular cutting method for silicon, but with Ultra low-K technology, using mechanical sawing will lead to various sawing defects such as chippings and delamination [1,2]. These leads to the introduction of Laser Grooving to get rid of these dilemmas. Laser grooving uses heat to eradicate metals on this very thin metal wafer dicing saw streets in preparation for wafer saw process to prevent topside chippings and delamination/metal peel off [3]. These defects are not acceptable especially since the product application is a chip

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card. Since chip cards must be flexible and durable, they require higher die and package strength to serve its purpose. To achieve such package requirement, different method was evaluated such as standard mechanical dicing, standard Laser Grooving and the PI laser groove.
The paper will discuss how we were able to achieve the quality requirement for Ultra Low-K and at the same time eliminating top reject contributor during startup of this device.

Keywords: Laser grooving; ultra low K; CMOS; PI grooving.

1. INTRODUCTION

The increasing demand of new technologies in the Semiconductor industry requires good customer satisfaction. Customer Satisfaction is the right word and the key factor in building good relationship with the customer. Any customer which will receive product failures, delay on their orders will reduce this satisfaction that latter results to business failure.

Wafer sawing is one of the preparatory processed of Integrated Circuit (IC) Back End manufacturing. As the part of the front operation, any scrappages will results to high loss of income since all wafers are being processed from the Front-End sites. Wafer Sawing need to have high-accuracy equipment. In addition, good wafer sawing starts on having an applicable saw blade with the proper combination to achieve good topside and backside cutting performance.

However, technology keeps going on to replace old school methodology. From the conventional mechanical sawing process using blades, an introduction of laser grooving was discussed on this paper. The introduction of this technology have mitigated the errors of mechanical blade sawing using blades which results to the achievement of increased process capability index.

2. LITERATURE REVIEW

2.1 The CHIP Card

A smart card is a flexible Plastic Card, usually made of PVC, that contains one or more embedded integrated circuits. The integrated circuit in a smart card is often referred as ICC, Smart Card Chip, Smart Chip Modules or Secure Microcontroller (Secure MCU) while the smart cards are often also referred as smartcards, chip cards, IC cards, ICC or CPU cards.

2.2 Ultra Low-K Silicon Technology

The demanding trend in the semiconductor resulted to complex wafer design and thinner metallization. The paper will focus on the 40nm wafer which is already considered an Ultra Low K which has the combination of Ultra Thick and Thin metals [4]. This technologies are used is mobile phone processor and Internet of Things (IoTs). However the presence of this Ultra Thick and Thin metals have trigger its suceptability to metal cracks, delmaination and chioppings which can results to diminished product performance.

Fig. 1. A sample of chip card

Fig. 2 shows an example the position of metal chippings that have been present on street with metalized scribe area. On the other hand, this phenomenon may affect the total die strength of the silicon die.

2.3 Major Issues during Qualification of CMOS E40 Ultra Low K Silicon Technology Using Mechanical Dicing

Fig. 3 shows several issues encountered during the start up which are related to silicon die fragility which inherent with the 40NM CMOS Ultra Low K Technology using mechanical blades sawing process.The material and process combination results to higher defect part per million occurrence.

2.4 Wafer Saw Pareto of Rejects Using Mechanical Blades

Fig. 4 shows the top rejects at Mechanical Wafer Sawing which are chippings, dangling and passivation cracks. Parameter optimization is one of the factor to be checked. Benchmarking for similar device to other sites were considered to have a base line on critical process parameters.

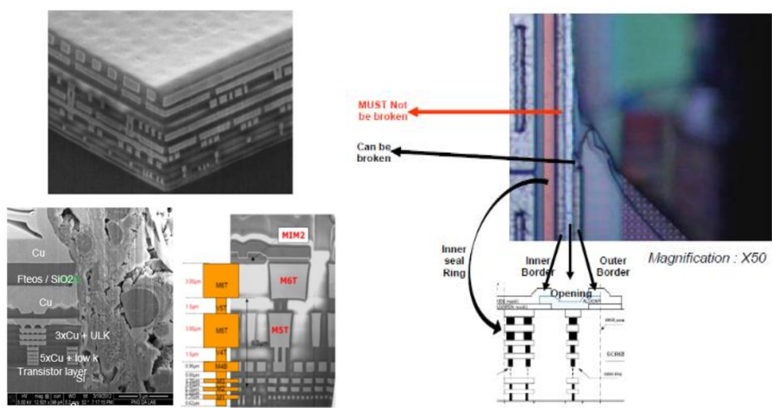

Fig. 2. Chipping/Peeling for 40NM CMOS Criteria

Board Ref #	Date	Customer	QTY IN	Rej	Fail type	Physical fail	Evidence
1	15-Aug	A	20	1	Card mute +O/S	Die crack	
2	26-Sep	A	20	1	Card mute +O/S	Crack in resine and wire cut	
3	22-Sep	B	10	1	Card mute +O/S	Suspect chip level delam and Die crack	
4	20-Sep	Internal Snap and replug trial (OSAT S)	500	16	Card Mute + O/S	Delam on wedge bond and Die cracked	
5	Oct 10	Internal Snap trial (no replug) (OSAT S)	100 (4 X 25) 2 Ops X 2 biadesive (Tesa vs Nitto)	2 from Op1 Both biadhesive s	Cards mute +O/S	Evidence of Chip level Delam and Die crack	

Fig. 3. Summary of Issues encountered during CMOS E40 lot start up

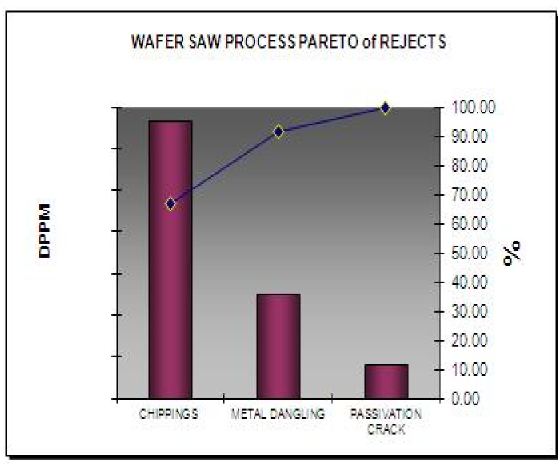

Fig. 4. 40 nm CMOS + Mechanical Wafer Saw Process Pareto of Reject

2.5 Risk Identifications

Critical risks were identified (Chart 1). Evaluation should be focused on these identified risks with the use of laser grooving, comparative study is needed. Baseline reference is the historical data acquired using mechanical blades. With collaborations and benchmarking, a laser grooving process was considered.

Further analyses and investigations of failures were made by collecting the actual reject samples from critical processes (Fig. 5).

Top rejects (based on Pareto) using mechanical dicing saw substantially affects the yield and quality of various product lines. Eliminating these defects are not possible through optimization and using different blade types (Fig. 6). Furthermore, it was established that these defects were related to the die technology (40nm CMOS), a very fragile Ultra Low-K silicon technology. A breakthrough solution was explored using laser grooving during wafer saw [5,6].

There are three factors that dominate the semiconductor technology process development: cost, performance, and form factor. The performance factor of wafer level driven by the front-end semiconductor foundries struggling to keep pace with “Moore's law.” The increased performance also requires thinner and improved “low-k” interlayer dielectric (ILD) materials.

However, these techniques present challenges for the mechanical integrity of the chips and introduce weakness in dies, which introduce yield loss, which greatly affect the manufacturing costs [7].

RISK ASSESSMENT

Item	Risks identified	Potential risk resulting from	Before Action			Considered Action
			Prob.	Impact	Class	
1	Frontside Chippings / Peeling	-Wafer Sawing Quality -Yield Loss -Relaibility	9	9	A	Use of Laser Grooving
2	Metal Dangling	-Wafer Sawing Quality -Yield Loss -Relaibility	9	9	A	Use of Laser Grooving
3	Passivation Cracks	-Wafer Sawing Quality -Yield Loss -Relaibility	9	9	A	Use of Laser Grooving

Chart 1. Wafer saw risk assessments

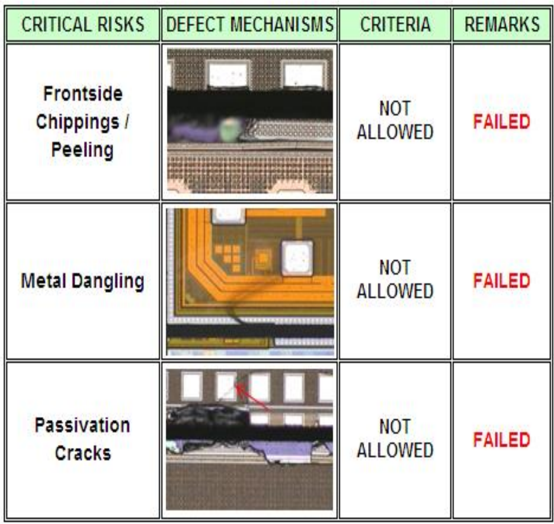

Fig. 5. Actual reject samples from critical processes

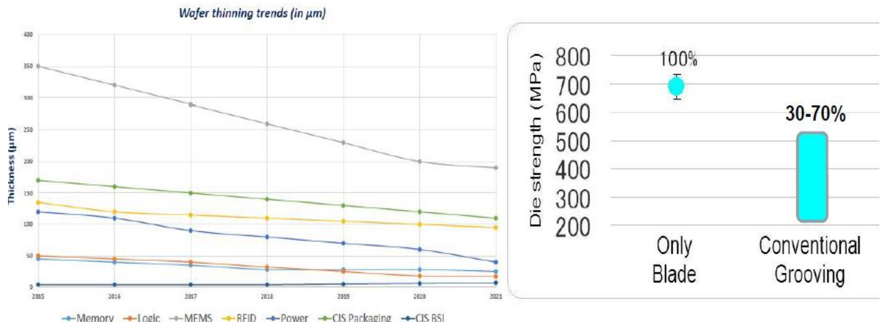

Fig. 6. Die Strength comparison between standard blade and conventional laser grooving.

3. EXPERIMENTATION

3.1 How Laser Grooving Works

Laser Grooving used the process of ablation [8,9] wherein the light of the laser goes through the solid medium. The higher intensity of laser light with respect to its threshold, the light will be converted into electrical, thermal, photochemical, and mechanical energy. The neutral atoms, molecules, positive and negative ions, radicals, clusters, electrons, and light are released explosively, and the surface of the substance is etch (Fig. 7).

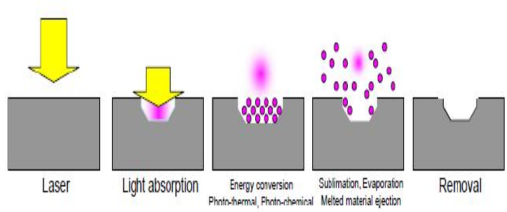

Fig. 7. Principle of Laser ablation

The condensed laser light emits an energy density over its defined threshold will be subjected to the media, results to ablation and latter cut. Process threshold and cut depth varies depending on the material. Fig. 8 shows the typical example of the threshold vs. the effect on the material.

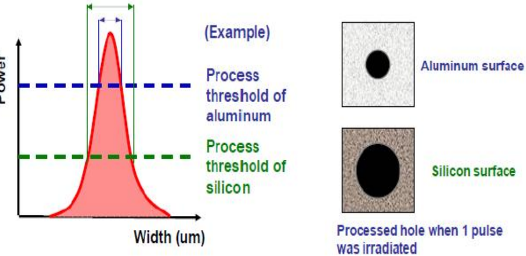

Fig. 8. Different Cutting Result vs. material

3.2 Methods of Laser Grooving

3.2.1 Standard laser groove

A process consists of two beams: narrow and wide beam (Fig. 9). Commonly three (3) pass combination of the narrow and wide beams were done depending on the material requirement [10].

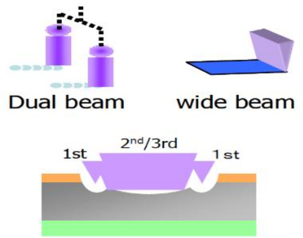

Fig. 9. Standard Groove Process

3.2.2 PI groove

A process of rapidly making two laser grooves in the dicing street –also known as "Pi Laser Grooving" (Fig. 10). The grooved dicing street will then be cut by mechanical blade (Fig. 11).

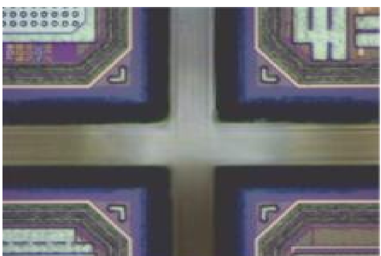

Fig. 10. Sample photo of Standard Groove after mechanical saw

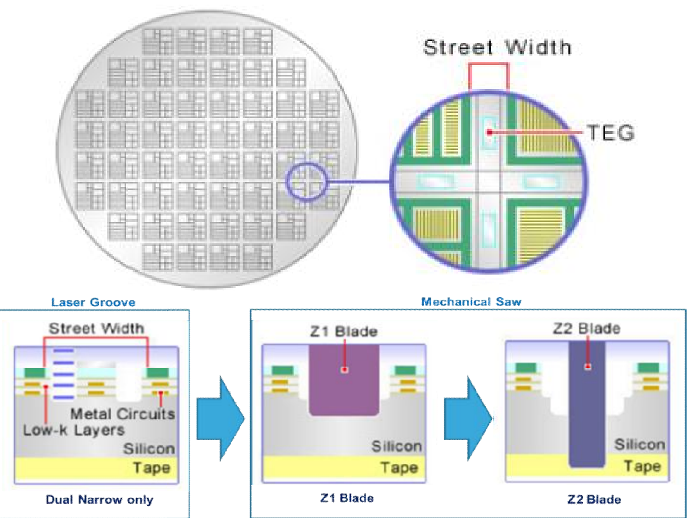

Fig. 11. Pi Groove Process

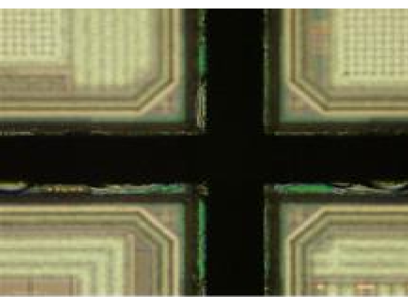

Fig. 12. Sample photo of Pi Groove after mechanical saw

3.2.3 Mechanical wafer dicing saw

Mechanical Wafer Blade saw [11] is a sawing process that involves a diamond blade installed in a spindle moving on high speed [12] which act as vertical grinder that helps wafer to cut semiconductor dies (Fig. 12).

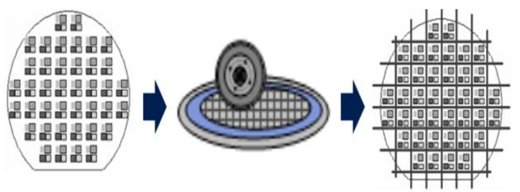

Fig. 13. Wafer Dicing Process

3.3 Design of Experiment

Design of experiments will focus on the variation of an older mechanical wafer saw compared to newer laser grooving process. The variation is to identify suitable process for Sim card IC which requires higher die strength. This DOE will focus on Laser Grooving parameters and its impact to three identified risks below.

Table 1. Process response qualification plan

Process steps	Product characteristics
A	Die Strength
B	Top Side Chippings
B	Back Side Chippings

Table 1 shows the critical process characteristics for laser grooving. As a main critical risk for SIM Card IC, die strength is considered for Laser grooving in order to check if the process will address the potential passivation cracks inherent to ultra-low-K silicon.

Table 2. Evaluation parameter (Power Setting) under process step A

Process Step (A)	Power Settings (W)
Leg 1	1.0
Leg 2	1.3
Leg 3	1.4
Leg 4	1.5
Leg 5	1.6
Leg 6	1.8

Table 2 are the legs identified with different power settings of Process Step A. The Power settings are for two narrow beams. Standard mechanical wafer sawing was also performed. The legs are defined based on its impact to metallization cut.

Table 3. Evaluation under process step B

Process Step (B)	Feed Speed (mm/sec)
Leg 1	Lower
Leg 2	Higher

Another critical parameter for laser grooving is the Feed Speed. Table 3 have defined two legs with different speeds. Lastly, all wafers will undergo automatic optical inspection (AOI) to screen out top side chippings and three point bend test for die strength response.

4. RESULTS AND DISCUSSION

4.1 Laser Grooving DOE Results

4.1.1 Die strength

Fig. 14 described the effect of different dual narrow beam power with respect to die strength response. One-way analysis shows that higher beam power results to minimized die strength which will not be suitable for SIM card IC.

Fig. 15 illustrates that 1.4 W power settings has the highest die strength values are maximum however resulted to 5% peeling defect rejection rate. Higher power settings resulted to a much more lower rejection rate and already becoming more constant. In order to balance the die strength and peeling defect rejection rate, 1.6W was identified as point of reference.

4.1.1.1 Top side chippings

One-way analysis with respect to Chippings, with an alpha of lower than 0.05, shows that there is a significant difference between the Laser grooving compared to mechanical dicing. Laser Grooving results to lower chippings with a maximum reading of 4 µm is observed. Therefore, Laser Grooving can mitigate the presence of top side chippings that latter can results to lower die strength.

An additional confirmatory test like Focused Ion Beam (FIB) was performed in order to have a cross-sectional view of the chipping attributed by laser grooving. Based on the FIB image, peeling was contained prior the seal ring and also confirms that no crack propagation was present inside the CMOS metallization.

4.1.2 Back side chippings

In order to also check the impact of mechanical dicing on Pi-grooved wafer, an evaluation of different lower, nominal, and higher settings was performed. All process wafers with Laser Grooving have very good chipping responses while the mechanical dicing, lower parameter setting resulted to backside chipping.

The identified POR for 40nm CMOS technology dies, Pi Grooving with 1.6W dual beam settings have been validated using the standard qualification process and all passed the reliability requirements of the package.

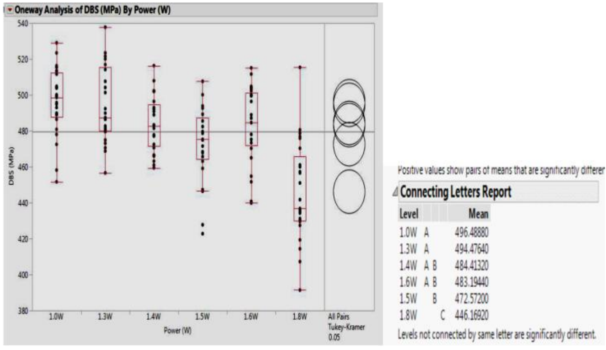

Fig. 14. Die strength response vs. Power settings

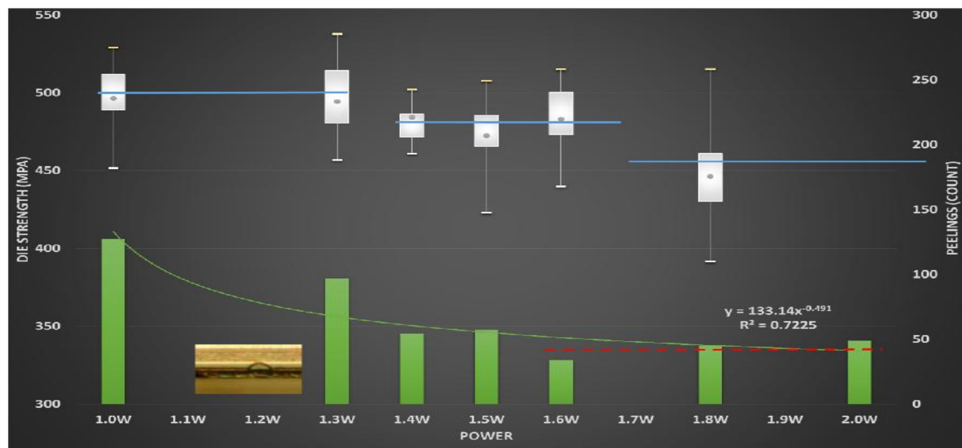

Fig. 15. Summary response for die strength response and Peeling/Chippings vs. Power settings.

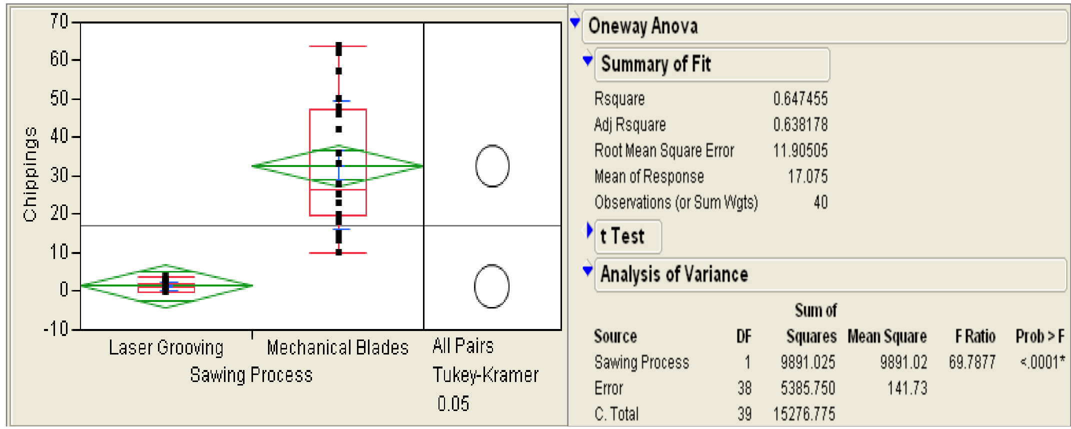

Fig. 16. Analysis of Variance (Laser Grooving vs. Mechanical Blade Sawing)

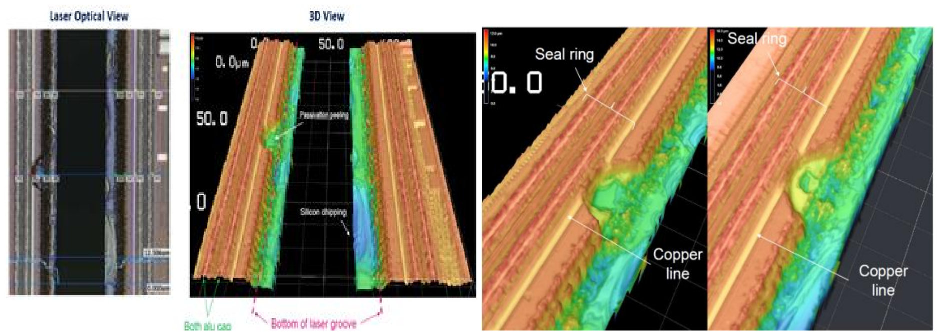

Fig. 17. 3D View of Chipping / peeling

Table 4. DOE Matrix for LMH parameters for Passivation Crack/Backside Chippings

	LL	LN	NN	NH	HH
Laser Grooving	Passed	Passed	Passed	Passed	Passed
Mechanical Dicing	Failed	Passed	Passed	Passed	Passed

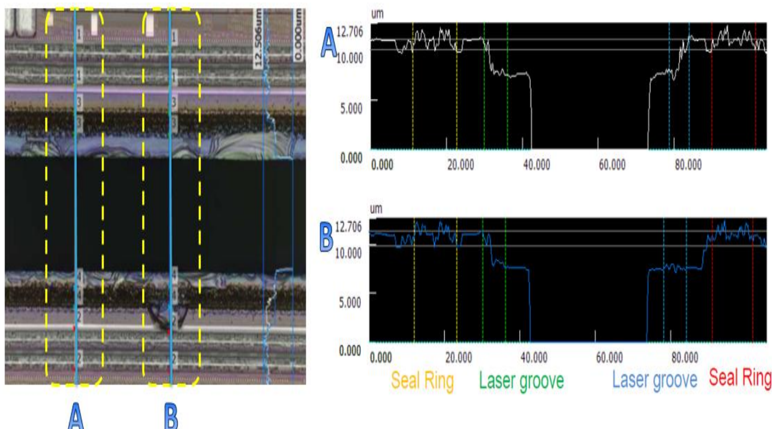

Fig. 18. Profile View of Sawn dice

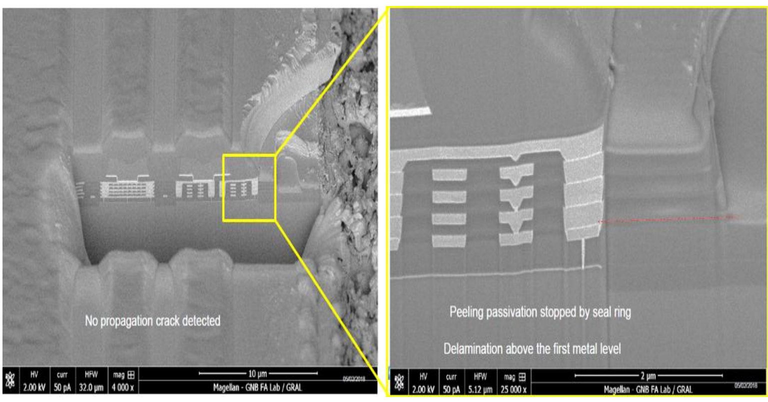

Fig. 19. FIB cross-sectional view of chippings / peeling

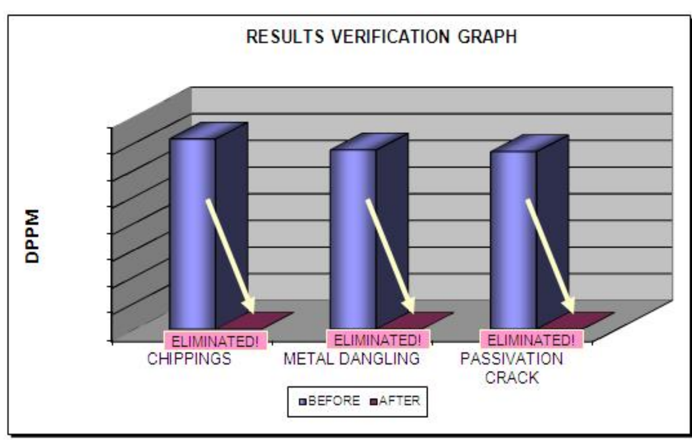

Fig. 20. Identified Risks Trend before and after the implementation of Laser Grooving. (Actual DPPM value were intentionally removed)

4.2 Large Scale Validation

After all qualifications and reliability were passed, large scale validation was executed to verify the defect per million impact of the newly identified process and its characteristics. Fig. 20 shows that Laser Groove with 1.6W Dual Beam settings have successfully

eliminated the three product characteristics: Chippings, Metal dangling and Passivation cracks.

5. CONCLUSION

The study shows that the demand for good customer satisfaction need a more focus response to define good process capability and product quality. The study has discussed the new silicon technology with Ultra Thick and thin metallization is in need for new process technology in order to mitigate the crucial product characteristics. The introduction of Laser Grooving and good design of experiments will help eliminate this potential quality concerns. Laser Grooving have also helped to increase the die strength requirement of SIM card integrated circuit. Laser Grooving which used light intensity to ablates the metallization will eliminates the cracks, which based on the study is where the lower die strength is propagating. Therefore, the help of Laser Grooving on increasing die strength results to higher flexibility of the integrated circuit embedded in the SIM card and latter its life expectancy.

6. RECOMMENDATIONS

It is recommended that the learnings gained using laser grooving be sustained and to continue the monitoring of its effectiveness until mass production mode. This project showed a robust solution in eliminating various sawing defects using state of the art technology as a breakthrough solution. This project showed how to dig and identify contributing factors on the top rejects by practical simulations and validations with the aid of statistical tools. This new technology of Laser Grooving is recommended to attain significant improvements and recommends a permanent fix to chronic wafer sawing issues. Learnings gained should be fanned-out and cross-fertilized to similar products/ technology. It is imperative that when new technology is coming in, critical processes are needed to be identified and that appropriate corrective actions and solutions be made so that when full production are set, deliveries will not be at stake.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Hsu HC, et al. An experimental study on dicing 28 nm low-k water using laser grooving technique. 9th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT); 2014.
2. Laurent P, et al. LowK wafer dicing robustness considerations and laser grooving process selection 8th Electronics System-Integration Technology Conference (ESTC); 2020.
3. Tu A, et al. Overcoming dicing challenges for low-k copper wafers using nickel-palladium-gold bond pads for automotive application. 14th Electronics Packaging Technology Conference; 2012.
4. AZO Materials. Wafer analysis of laser grooving. Available:https://www.azom.com/article.aspx?ArticleID=18277
5. Lie H, et al. Investigation of 3-pass laser grooving process development for low-k devices. 17th Electronics Packaging and Technology Conference (EPTC); 2015.
6. Shie KW, et al. Single & multi beam laser grooving process parameter development and die strength characterization for 40 nm node Low-K/ULK wafer. 16th Electronics Packaging Technology Conference (EPTC); 2014.
7. Bacquian, Bryan Christian S. Dicing before grinding: A robust wafer thinning and dicing technology. Journal of Engineering Research and Reports; 2020.
8. DISCO Corporation. Ablation Process. Available:https://www.disco.co.jp/eg/solution/library/laser/ablation_process.html
9. Savriama, Guillaume. Review of laser technologies for dicing microelectronics chips. Research Gate; 2016.

10. Richard VDS, et al. Multi beam low-k grooving evaluation of various removal principals. 46th International Symposium on Microelectronics; 2013.
11. DISCO Corporation. Electroformed bond hub blades – high performance hub blades that take on the challenges of cutting. Available:https://www.disco.co.jp/eg/products/catalog/pdf/nbczh.pdf
12. DISCO Corporation. Fully automatic dicing saw – advanced performance for 300 mm dicing. Available:https://www.disco.co.jp/eg/products/catalog/pdf/dfd6361.pdf

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